Title: Oscillator circuit and an oscillator biasing method.

The invention relates to an oscillator circuit. The invention further relates to an oscillator biasing method.

Integrated oscillators are used as frequency references in all kind of integrated circuits, especially integrated synthesisers and integrated transceivers. The reduction in power consumption in these oscillators is of prime-importance in application with a limited power supply, such as a battery. Usually the design of an oscillator is based on phase-noise requirements, minimum amplitude or minimum required negative-resistance in order to sustain oscillation.

It is therefore a goal of the invention to provide an oscillator circuit with a low power consumption. In order achieve this goal, according to the invention an oscillator circuit , at least comprising: at least one oscillator device with a first oscillator contact and a second oscillator contact, and a bias voltage source having a first source contact connected to said first oscillator contact and a second source contact connected to said second oscillator contact, wherein said bias voltage source includes a varying voltage source which in use provides a bias voltage varying in time.

The oscillator circuit has a low power consumption, because the bias voltage source is a varying bias voltage source. The time averaged bias voltage of a varying bias voltage of a certain (maximum) amplitude is lower than the bias voltage of a DC bias source with the same amplitude. The current flowing through the circuit is proportional to the average bias voltage and hence the current consumption is lower. The lower current consumption causes a lower power consumption, since the consumed power is equivalent to the product of the current and the voltage.

The invention further provides an oscillator biasing method according to claim 15.

Specific embodiments of the invention are set forth in the dependent claims.

Further details, aspects and embodiments of the invention will be described with reference to the attached drawing.

Fig. 1 shows a block diagram of a first example of an embodiment of an oscillator circuit according to the invention.

Fig. 2 shows a circuit diagram of a second example of an embodiment of an oscillator circuit according to the invention.

Fig. 3 shows a block diagram of a first example of a bias voltage source for in an oscillator circuit according to the invention.

Fig. 4 shows a circuit diagram of a second example of a bias voltage source for in an oscillator circuit according to the invention.

Figs. 5 shows a graph of the simulated temporal development of the voltage at node outp in the example of fig. 2 .

Figs. 6 shows a graph of the simulated temporal development of the voltage at node inp in the example of fig. 2 .

Figs. 7 shows a graph of the simulated temporal development of the voltage at node Vcm in the example of fig. 2 .

Fig. 8 shows a graph of the simulated temporal development of the current consumption of the example of fig.1.

Fig. 1 shows a example of an embodiment of an oscillator circuit 1 according to the invention. The oscillator circuit 1 comprises an oscillator device 100, a limiter or clipper device 101 and a bias voltage source Vbias. The oscillator device 100 is connected to the limiter device 101 via a first oscillator contact inp and a second oscillator contact inn. The limiter may also be connected to the oscillator via a different number of contacts, such as a single contact or three or four contacts. The resonator 100 is connected to a bias voltage source Vbias via an oscillator bias input Vcm. The limiter device has a first limiter output contact outp and a second limiter output contact outn. The limiter may have a different number of output contacts, such as for example a

single output contact or three or four output contacts. In the shown example, the outputs outp,outn of the limiter device 101 constitute outputs of the oscillator circuit 1.

In use, the oscillator 100 generates an oscillating signal, such as a sine-wave, a square wave or a saw-tooth wave. The oscillator 100 presents the oscillator signal at each of the oscillator contacts inp, inn. In the example, if is assumed that the signal at the first oscillator contact inp has a phase difference of substantially 180 degrees with respect to the signal at the second oscillator contact inn, i.e. they are substantially in antiphase. However, there may likewise be other phase differences or no phase difference between signals at the oscillator contacts.

The limiter device 101 acts as a signal shaper and may be replaced with another signal shaper device, such as for example a band-pass filter, a switch or otherwise.

The oscillator signal is received by the limiter device 101 which performs a limiting or clipping function. In general, the terms limiter and clipper are synonymous and are used interchangeable in this application without limitation to the functions and/or properties of the limiter or clipper device. The limiter automatically sets at least one boundary value upon the oscillator signal, i.e. if the amplitude of the oscillator signal exceeds the boundary signal, the signal is distorted. In the shown example, the limiter device 101 outputs a limiter output signal with an amplitude proportional to the oscillator signal as long as the oscillator signal has an amplitude below the boundary value and outputs a signal with a constant amplitude when the amplitude of the oscillator signal is above the boundary signal. Thus, if the input signal has an amplitude above the boundary value, the limiter output signal of the limiter device is clipped, i.e. the limiter output signal is constant and more or less independent from the input signal. If the amplitude of the oscillator signal is below the boundary value, the output signal of the limiter

device is not clipped anymore and becomes substantially proportional to the oscillator signal.

The clipped signal is presented at the first limiter output outp and a 180 degrees phase shifted signal is presented at the second limiter output outn. However, other phase differences or no phase difference between signals at the limiter contacts are likewise possible. For example in quadrature applications with image rejection a 90 degrees phase difference may be appropriate.

The oscillator 100 is biased by a bias voltage from the bias voltage source Vbias. In the example of fig. 1 the bias voltage source Vbias provides a square wave bias voltage. That is, the bias voltage has either a value V_1 or a value V_2. When the bias voltage is equal to V1, the bias voltage source is in a first state, and when the bias voltage is equal to V2, the source is in a second state. In the example of fig. 1, V2 is equal to zero and V1 a positive value. Thus, in the first state the bias voltage is on and in the second state the bias voltage is off.

If the bias voltage source Vbias is turned on, i.e. the bias source is in the first state, the oscillator device 100 starts oscillating. After some time the bias voltage is switched off. The bias source Vbias is then in the second state. Due to the energy stored in the oscillator the oscillator will keep on oscillating. However, the amplitude of the oscillator will decrease in time because of the losses present in every real oscillator. Before the oscillator signal reaches an amplitude at which the limiter stops functioning properly, the bias voltage source is switched on again.

Because the bias voltage is turned off for some period of time, the power effectively used by the oscillator circuit is lowered compared to a DC bias voltage. Furthermore, the amplitude and shape of the output signal of the oscillator circuit do not change because of the limiter device 101. Instead of switching the bias voltage off, it is also possible to switch the bias voltage from a high state to a lower state, i.e. to set V2 to a non-zero value which is lower

than V1. Thereby, the decrease of the oscillator signal amplitude will be slower.

Instead of the bias voltage source, a bias current source with a varying current source which in use provides a bias current varying in time may be used.

Fig. 2 shows an electrical circuit of a second and more detailed example of an oscillator circuit 10 according to the invention. The oscillator circuit 10 comprises an oscillator device 100 connected to a limiter device 101 via oscillator contacts inp,inn. The oscillator device 100 is further connected with the oscillator contacts inp,inn to a negative resistor or amplifier device 102. The oscillator device and the negative resistor 102 are also connected to a bias voltage source via a bias voltage contact Vcm and ground gnd. A pulse current source Istart is placed between the oscillator contacts to help the oscillator start oscillating in a simulator. In practice, , noise present in the circuit may start the oscillator and the pulse current source may be omitted

The oscillator device 100 comprises a first inductance Lresa and a second inductance Lresb connected in series. A capacitance Cres is connected in parallel to the inductances Lresa,Lresb. A resistor Rloss is connected in parallel to the capacitance Cres. The resistor Rloss represents losses in the oscillator, i.e. losses the inductors and/or the capacitor. In a physical implementation of the invention, the resistor may be omitted, since in reality the inductors and/or capacitors exhibit always some resistance.

The oscillator device 100 is a parallel LC-resonator, as is generally known in the art of oscillators. The LC-resonator has a mode of oscillating with a resonance frequency. The resonance frequency is also called the fundamental frequency of the oscillator. The resonance frequency is determined by the capacitance Cres and the inductances Lresa, Lresb, as is generally known in the art. The resonance frequency may mathematically be described by:

$$fres = \frac{1}{2\pi\sqrt{(Lresa + Lresb)Cres}} \qquad (1)$$

In equation (1) *fres* is the series resonance frequency and *Lresa, Lresb* and *Cres* are the reactances of the inductors Lrfesa, Lresb and the capacitor Cres respectively.

The oscillator 100 is biased by a bias voltage from the bias voltage source Vbias. The bias voltage source outputs a varying signal, in this example a square wave signal as is explained above with reference to the bias voltage source in fig. 1. Thus the oscillator circuit 10 of fig. 1 only consumes power if the voltage source Vbias is turned on. Hence, the power consumption of the oscillator circuit 10 is low.

Furthermore, the phase-noise of the oscillator circuit 10 is improved when the bias voltage source Vbias is switched off. As is known from C.A.M. Boon, "*Design of High-Performance Negative-Feedback Oscillators*", Ph.D.Thesis, Delft University of Technology, Delft, The Netherlands, 1989, the phase noise CNR of an oscillator may be described by the mathematical equation:

$$CNR = \frac{kTF}{P_{res}Q^2}\left(\frac{f_0}{\Delta f}\right)^2 \qquad (1)$$

where k denotes the Boltzman constant, T is the absolute temperature, F is the Noise Factor of the active part of the oscillator compared to the noise of the resonator, P_{res} is the power dissipated in the resonator, Q is the resonator quality factor, f_0 is the oscillation frequency and f is the offset frequency at which the phase-noise is measured. In practice the Noise Factor F is in the order of 2 to 3 (6 to 10 dB) for properly designed oscillators. In the case that the bias voltage source is switched off, the noise of the active circuitry decreases because there is less active circuitry. As a consequence, the Noise Factor F in equation (1) decreases to 1 (0 dB). Thereby, the Carrier-to-Noise Ratio even increases if the power in the oscillator does not drop to more than a factor of 2 to 3, or a decrease in amplitude, which is equal to the square root of the power, of 2 1.4 or 3 1.7.

The negative resistor or amplifier device 102 compensates for losses in the oscillator 100, for example those represented by the resistor Rloss. The amplifier device 102 comprises a first transistor Mresa and a second transistor Mresb. In fig. 2 the transistors are MOS (Metal Oxide Semiconductor) transistor devices. A drain d_a of the first transistor Mresa is connected to the second oscillator contact inn. A drain d_b of the second transistor Mresb is connected to the first oscillator contact inn. The sources s_a,s_b and the back-gates b_a,b_b of the transistors Mresa,Mresb are connected to ground. The gate g_a,g_b of each of the MOS transistor device Mresa, Mresb are connected to the drain d_a,d_b of the other MOS transistor device Mresa, Mresb, so the transistors are cross-connected.

Each of the transistors Mresa,Mresb outputs a current at its drain proportional to a voltage difference between its gate and its source. Thus, the output current of transistor Mresa is proportional to the voltage difference between the first oscillator contact inp and ground and the output current of the transistor Mresb is proportional to the voltage difference between the second oscillator contact inn and ground. For example, if the voltage at the first oscillator contact inp is low, the voltage at the second oscillator contact inn will be high in case of a 180 degrees phase shift. The second transistor Mresb will then inject a current towards ground, thus lowering the voltage at the first oscillator contact further thereby driving the oscillator. The first transistor Mresa operates in a similar manner with respect to the other contact.

Also connected to the first oscillator contact inp is a first limiter transistor Mlima, while a second limiter transistor Mlimb is connected with its gate to the second oscillator contact inn. The drain of each of the limiter transistors is connected to a limiter resistor Rlima resp. Rlimb. The source of the limiter transistors are connected to each other and to a bias current source Ibias. The limiter transistors, resistors and the bias current source form a differential amplifier stage 101. In use, the bias current of the bias current

source Ibias is such that the amplifier is in overdrive if at the input a signal with amplitude equal to the minimal amplitude of the oscillator signal is presented. The minimal amplitude of the oscillator signal is the amplitude thereof, just before the bias voltage source is turned from the lower state to the second state. The differential amplifier thus acts as a limiter, i.e. the output signal is always clipped if the input signal of the differential amplifier exceeds the minimal amplitude. Instead of a differential amplifier any other limiter device may be used, such as a switch or a (bandpass) filter, to obtain a time-invariant amplitude of the oscillator circuit output signal.

The bias voltage source in figs. 1 and 2 outputs a square wave voltage signal. The generation of a square wave signal is generally known in the art and the bias voltage source may be of any type appropriate in the specific implementation. The bias voltage source may be an analogue or a digital device. Instead of a square wave, the bias voltage source may generate a different varying signal. Fig. 3 an fig. 4 show examples of a bias voltage source which may be implemented in an oscillator circuit according to the invention.

The example of fig. 3 comprises a voltmeter device Meas connected to oscillator contacts inp,inn. The meter Meas is connected to a threshold device Tr. The threshold device Tr is connected to a control input S1 of a switch device S. A first switch contact S3 is connected to a DC bias voltage source Vdc. The DC bias source Vdc is also connected to ground. A second switch contact S2 of the switch S is connected to the bias input contact Vcm.

In a conducting state, the switch contacts S2,S3 are electrically connected to each other and in a non-conducting state, the switch contacts S2,S3 are electrically disconnected. Thus, if the switch is in the conducting state, the voltage difference between the bias contact Vcm and ground is substantially equal to the bias voltage, while in the non-conducting state no bias voltage is applied to the bias contact. The state of the switch S is controlled by a signal outputted by the threshold device to the switch controlinput S1.

The meter Meas measures a voltage difference over the oscillator contacts and transmits the measured difference to the threshold device Tr. The threshold device Tr compares the measured voltage with a predetermined voltage threshold. If the measure voltage is above the threshold, the threshold device Tr outputs a signal representing a binary one, if the measure voltage is below the threshold, the threshold device outputs a signal representing a binary zero. Thereby, if the measure voltage is below the threshold, the switch is put in the conducting state and if the measure voltage is above the threshold the switch is put in the non-conducting state. The bias voltage is thus automatically turned on and switched off depending on the signal outputted by the oscillator device.

In the bias voltage source of fig. 4, a bias resistor Rbias and a bias capacitor Cbias connected in series are placed between the first oscillator contact inp and the second oscillator contact inn. A discharge resistor Rdis is connected in parallel to the capacitor Cbias. The discharge resistor Rdis is connected to the node between the bias resistor and the bias capacitor and the second oscillator contact. A bias diode device Dbias is connected in series with the resistor Rbias. The bias diode device has a first diode contact connected to the first oscillator contact inp and a second diode contact connected to the resistor Rbias.

If the first diode contact is more than a diode voltage above the second diode contact the bias diode device Dbias is in a forward state. The bias diode device is in reverse, that is in a substantially non-conducting state if the voltage difference between the first diode contact is less than the diode voltage above the second diode contact or the voltage of the first diode contact is below the voltage of the second diode contact. The bias diode acts as a peak detector for measuring the amplitude of the oscillator signal, since the diode will be in forward if the voltage difference over diode contacts exceeds the diode voltage. Therefore, the diode only conducts above a certain amplitude of the voltage

difference over the diode contacts, which is related to the signal applied at the first and second oscillator contact inp, inn.

The gate of a bias transistor Mbias2 is connected to the node between the bias capacitor Cbias and the bias resistor Rbias. The source of the transistor Mbias2 is connected to a power supply Vccand the drain of the transistor Mbias2 is connected to the bias contact Vcm.

If a voltage is applied over the oscillator input contacts inp,inn, the bias capacitor Cbias will be charged, resulting in a voltage rise over the bias capacitor contacts, and thus resulting in a voltage rise at the bias resistor- bias capacitor node with respect to ground. The voltage at the bias resistor- bias capacitor node controls the state of the second bias transistor Mbias2. Thus, if the voltage at the node has reached a certain value the second bias transistor Mbias2 opens. If the second bias transistor Mbias2 is closed a voltage difference will exist between the source and drain of the second bias transistor Mbias2. Thereby the bias of the oscillator is turned off. Because the oscillator bias is turned off, the bias capacitor Cbias will not be charged anymore. The discharge resistor Rdis will slowly discharge the bias capacitor Cbias, thereby lowering the gate voltage of transistor Mbias2. After some time, the transistor Mbias2 will be switched on again, thus restarting the complete cycle.

The moment of opening and closing of the bias transistor may be adjusted using appropriate circuitry and will be apparent to a person skilled in the art of electronics.

The bias voltage source may also be implemented in a way different from the example shown in figs. 3 and 4. For example, the bias signal may be generated with a DC current source connected to one input of an edge triggered bistable device (also known as flipflop) and a clock signal supplied to both a the second input and the clock signal of the input. The bias signal may be generated in any other way, for example by counting the number of pulses from a clock. When the number of counted pulses is below a first predetermined value N, the output signal is high and if the number of counted

pulses is above the first predetermined value N but below a second predetermined value M the ouput signal is low. The duty cycle is then equal to N/M, that is the ratio of the time the bias current has a high value (V_1) and the total signal period. Furthermore, the bias voltage may be of any non-DC signal type, such as a sine wave signal, saw tooth signal or any other type of signal.

Due to the lower amplitude driving the limiter after the bias voltage is switched off, the output signal of the limiter may have less steep rise- and fall-slopes. The oscillator circuit may be provided with a second limiter device to increase the steepness of the slopes . The second limiter device may for example be connected to the limiter output of the first limiter device, i.e. the limiters may be connected in series. In that case, for example one or more output contacts of the second limiter may be used as the output contacts of the oscillator device.Instead of the oscillator shown in fig.2, any other type of oscillator or resonator may be used in the oscillator circuit. The oscillator may for example compre electronic components forming an oscillator circuit, such as a series LCR oscillator or an inverted loop oscillator, or the oscillator may be a physical oscillator or resonator body, such as a tuning fork, a cavity resonator, a piezo-electric crystal, a rhumbatron or an acoustic oscillator, as are generally known in the art.

Figures 5-8 show graphs of a simulated performance of the oscillator circuit of fig. 2. In the simulation, the values of the inductances Lresa,Lresb and the capacitance Cres are chosen such that the oscillator has a resonance frequency of 1 MHz. The bias voltage source is assumed to be a squarewave AC bias voltage source with a duty cycle of 28 % and a period of 25 microseconds. The bias voltage is switched between 0 and 1V. The values of the components are listed in table 1. The transistors were simulated to be Metal Oxide Semiconductor (MOS) transistors with a width of 100 μm and a length of 0.35 μm.

Table 1

Lresa	Lresa	Cres	Rloss	Rlima	Rlimb	Vcc	Vbias	Ibias
800nH	800nH	15.8nF	1k	10k	10k	2V	V1=1 V V2=0 V	100 A

As is shown in fig. 5, the bias voltage is turned on 5 microseconds after starting the measurement, as is indicated with dotted line A. Six microseconds later the bias voltage is turned off, as is indicated with dotted line B. At t=30 microseconds, the bias voltage is switched on again and at t=36 microseconds the bias voltage is turned off. At the moment the bias voltage is switched on for the first time, the oscillator is already oscillating, as is shown in fig. 6. The oscillator continues oscillating but with a DC voltage added to the voltage difference between the oscillator contacts. The DC component disappears when the bias voltage is turned off. Note that the DC component does not affect the limiter device as the limiter has a high Common-Mode rejection. The output of the oscillator circuit, which is the signal presented at the limiter outputs outp,outn does not change in time and is independent of the bias voltage, as is shown in fig. 7. It is a square-wave with a fixed amplitude, and has the frequency of the oscillator.

In fig. 8 the current consumption of the oscillator circuit 10 is shown, As can be seen, the circuit only consumes current (and hence consumes only power) when the bias voltage is turned on, i.e. between t=5 and 12 microseconds and t=30 and 37 microseconds. The current consumption is approx. 14 mA when the bias voltage is on. The average current consumption is approx. 2.4 mA in this example. This is approx. 6 times lower compared to the case when the oscillator would be ON continuously.

An oscillator circuit according to the invention is particularly suited for use in an integrated circuit because of its reduced power requirements. In general, integrated circuits are smaller, have a lower power consumption and improved performance characteristics compared to circuits comprising discrete

components and are widely used in small portable devices fed by a power cell, which may be charged from time to time. Low power requirements result in increased standby and operational periods between charging moments. In battery operated applications, such as for example mobile phones, wireless device operating in accordance with the Bluetooth protocol, handheld computers and laptop computers, a long battery life time is of prime importance. Furthermore, if an oscillator circuit according to the invention is used is such an application the battery capacity or battery size may be reduced.

Such an integrated circuit may be manufactured in a CMOS process, which in general provides a small device with a low power consumption.

An oscillator circuit according to the invention is also especially suited for implementation in wireless device with limited power supply and/or which size should be as small as possible, such as mobile telephones or devices communicating via the so called Bluetooth protocol. It should be noted that the oscillator circuit may also be implemented with at least one discrete component.

Furthermore, an oscillator circuit according to the invention may be implemented in a receiver device or a transceiver (transmitter and receiver) device. A receiver device is an electronic device for the reception and processing of electro-magnetic signals such as radio signals. A transceiver device is a receiver device which is able to transmit electro-magnetic signals as well.

A receiver device or a transceiver device with an oscillator circuit according to the invention may be used in any wireless electronic device. A wireless electronic device is any device used for the reception of electro-magnetic signals. A wireless electronic device may comprise a transmitter functionality for the transmission of electro-magnetic signals. The wireless electronic device may for example be a device with a limited power supply (such as a battery), such as mobile telephone, a portable radio or a lap-top

computer connected to a other device via a Bluetooth connection. The wireless electronic device may, however, also be a device with a virtually unlimited power supply, like a mobile telephone base station or a desktop computer communicating to other device via a Bluetooth connection.

5

CLAIMS

1. An oscillator circuit (1), at least comprising
at least one oscillator device (100) with
at least one oscillator bias contact (Vcm)
and
a bias source (Vbias) having a source contact connected to said oscillator bias contact,
wherein
said bias source includes a varying bias source which in use provides a bias varying in time.

2. An oscillator circuit (1) as claimed in claim 1, wherein said bias source is a switched DC source which in use provides a bias signal varying between a first level and a second level.

3. An oscillator circuit (1) as claimed in claims 1 or 2, further comprising a signal shaper device (101) connected to an oscillator output contact of said oscillator device.

4. An oscillator circuit (1) as claimed in claim 3, wherein said signal shaper device comprises at least one limiter device (101).

5. An oscillator circuit (1) as claimed in claim 3, wherein said signal shaper device comprises a band-pass filter device.

6. An oscillator circuit (1) as claimed in any one of the preceding claims, further comprising:
a bias control circuit (Meas,Tr,S) for switching the bias source (Vbias) on and off depending on a signal outputted by the oscillator device (100).

7. An oscillator circuit (1) as claimed in any one of the preceding claims, wherein said oscillator device (100) at least comprises at least one electrical device with a positive feedback loop.

8. An oscillator circuit (1) as claimed in any one of the preceding claims, wherein said oscillator device (100) at least comprises at least one resonator body.

9. An oscillator circuit (1) as claimed in any one of the preceding claims, further comprising a negative resistance device (102) at least comprising at least one transistor device (Mresa,Mresb).

10. An oscillator circuit (1) as claimed in claim 4, wherein said limiter (101) at least comprises at least one differential amplifier (Mlima,Mlimb) with:
at least one input contact connected to at least one oscillator output contact (inp), and
at least one output contact (outp) connected to a load.

11. An oscillator circuit (1) as claimed in claim 10, wherein said load comprises:
at least one resistor (Rlima) connecting at least one of said at least one output contacts (outp) to a power supply (Vcc).

12. An oscillator circuit (1) as claimed in any one of the claims 4-11, wherein said limiter (101) at least comprises at least one transistor device (Mlima, Mlimb).

13. An oscillator circuit as claimed in any one of the preceding claims, wherein said bias source comprises a bias voltage source.

14. An oscillator circuit as claimed in any one of the preceding claims, wherein said bias source comprises a bias current source.

15. An oscillator biasing method, at least comprising:
applying a bias over a first oscillator bias contact (Vcm);
switching said bias off if a predetermined first criterion is satisfied and switching said bias on if a predetermined second criterion is satisfied.

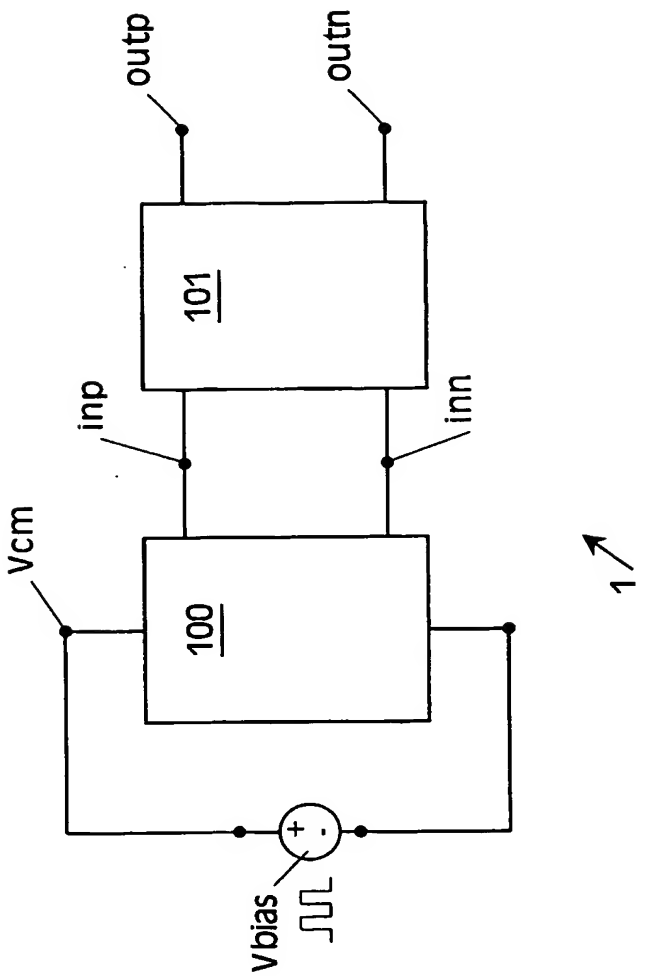
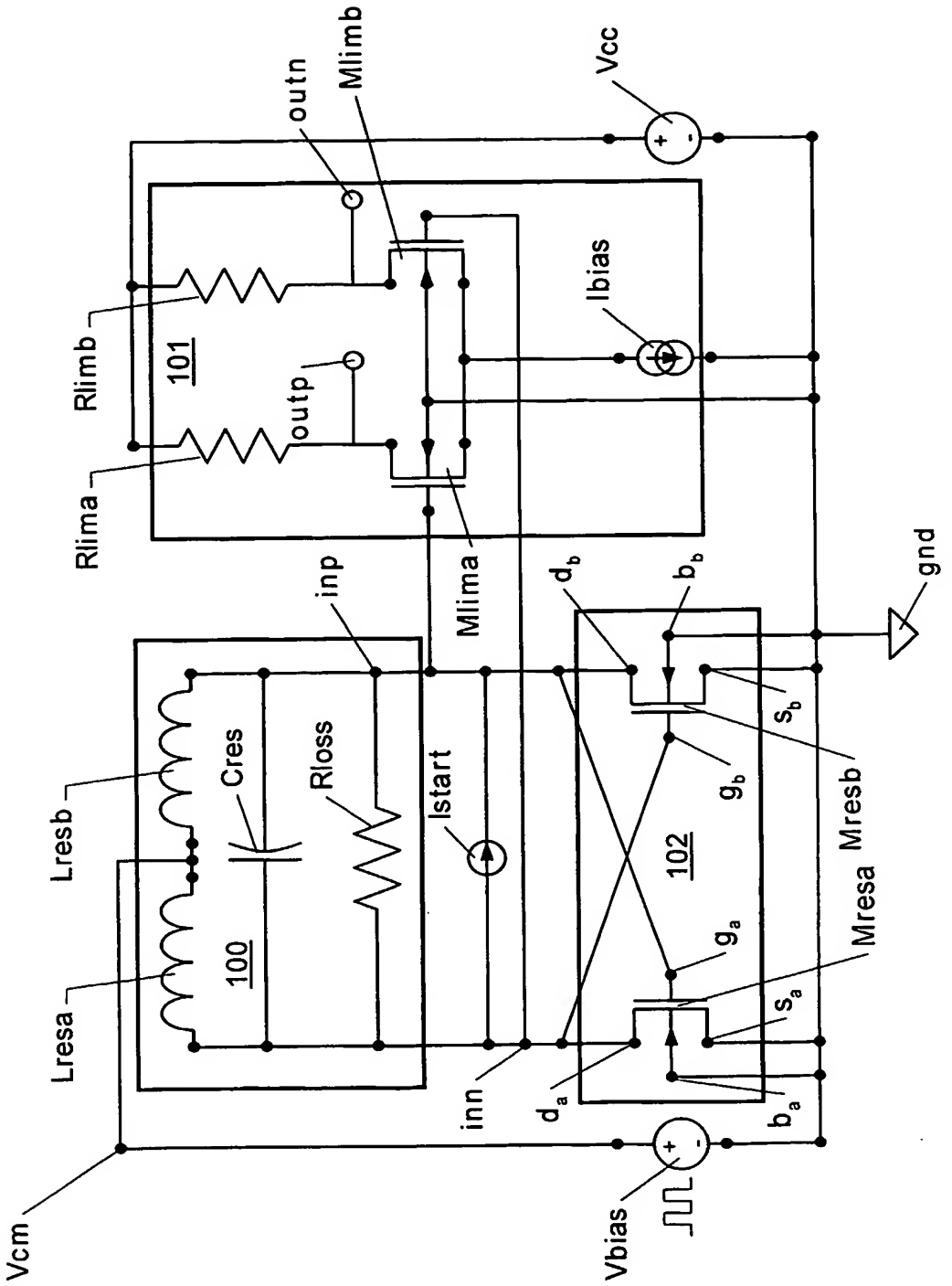


Fig. 1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Mlimb
Vcc
Rlimb
101
outp
Ibias
Rlima
Mlima
inp
d_b
b_b
gnd
Lresb
Cres
Rloss
Istart
s_b
g_b
Mresb
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g_a
Mresa
Lresa
100
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inn
d_a
b_a
Vcm
Vbias
10

Fig. 2

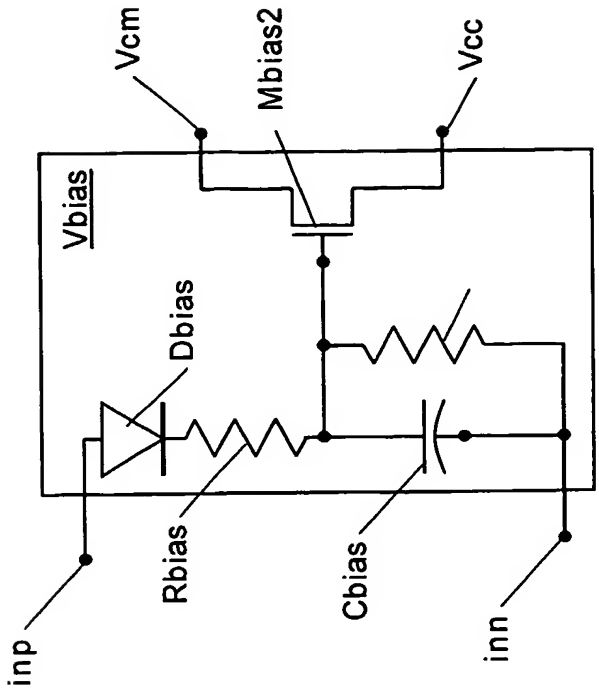
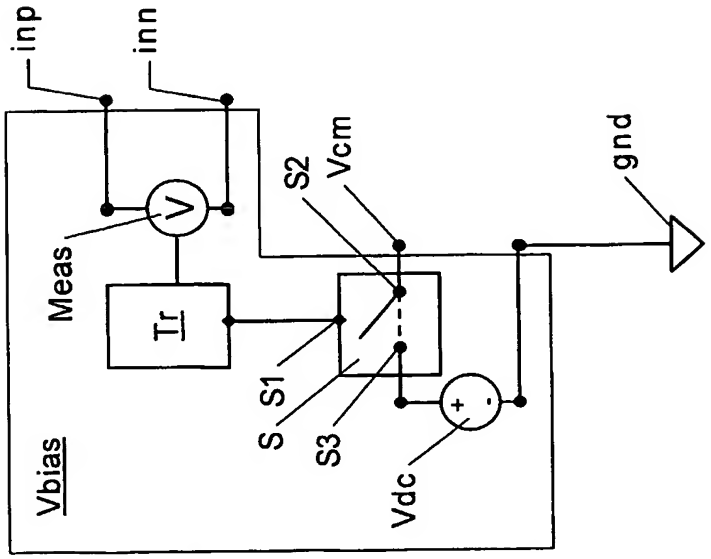

Vcm
Mbias2
Vcc
Vbias
Dbias
Rbias
Cbias
inp
inn

Fig. 4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inn
S2
Vcm
gnd
Meas
V
Tr
S1
S
S3
Vdc
Vbias

Fig. 3

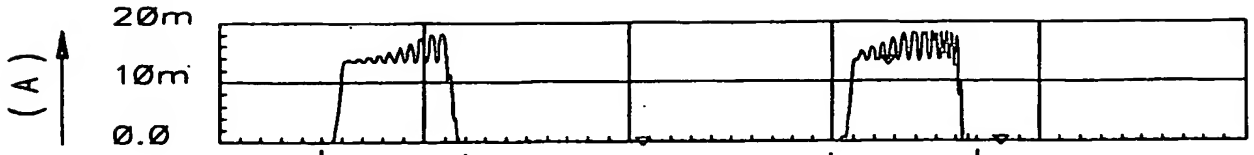

Fig. 8

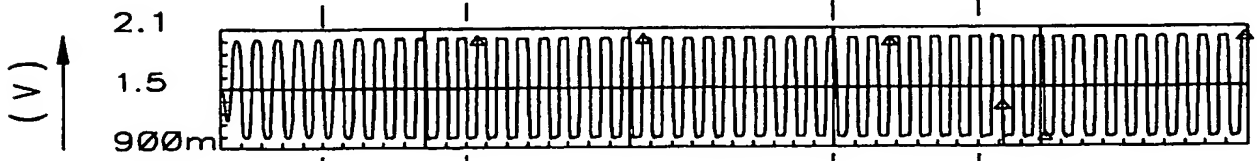

Fig. 7

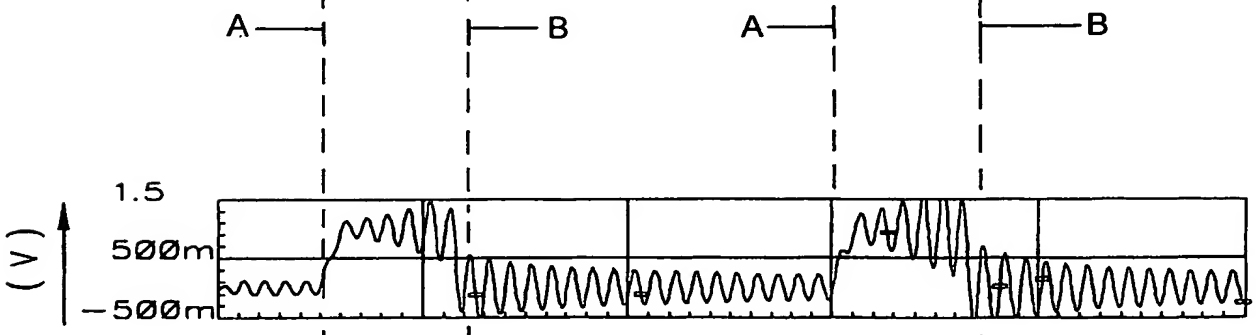

Fig. 6

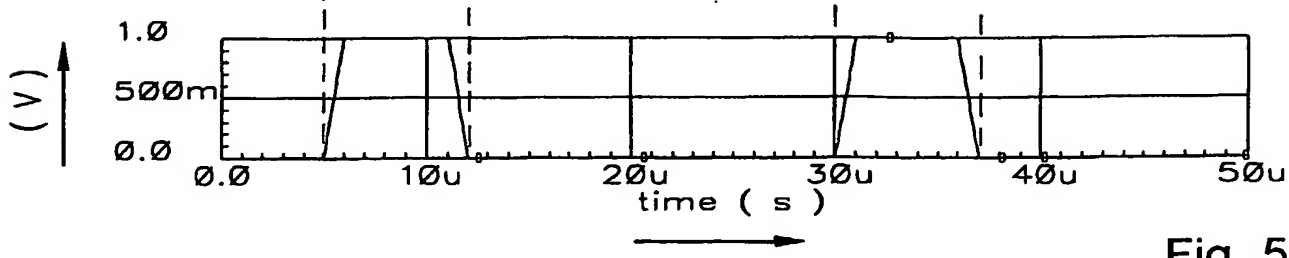

Fig. 5

INTERNATIONAL SEARCH REPORT

PCT/NL 02/00221

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03B5/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC, COMPENDEX, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 3 979 693 A (SAARI VEIKKO REYNOLD) 7 September 1976 (1976-09-07) abstract; figure 1 column 2, line 26 - line 32 column 3, line 3 - line 7 column 3, line 48 - line 56 column 3, line 63 - line 65 column 3, line 67 -column 4, line 2 column 4, line 11 - line 16 column 5, line 62 -column 6, line 2 figures 2,3	1-15
X	US 4 590 513 A (CRAFT JACK) 20 May 1986 (1986-05-20) abstract; figure column 4, line 2 - line 4	1-15

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[X] Further documents are listed in the continuation of box C.

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12 November 2002	19/11/2002

Name and mailing address of the ISA	Authorized officer
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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